REMARKS

Please reconsider the application in view of the following remarks. Applicant thanks the Examiner for carefully considering this application.

Disposition of Claims

Claims 1-36 are pending in this application. Claims 1, 10, 19, and 28 are independent. The remaining claims depend, directly or indirectly, from claims 1, 10, 19, and 28.

Rejection(s) under 35 U.S.C § 103

Claims 1-9 and 19-36 stand rejected under 35 U.S.C. § 103 as obvious over U.S. Patent No. 6,446,188 ("Henderson") in view of U.S. Patent No. 6,240,484 ("Witt"). This rejection is respectfully traversed.

Claim 1 recites a computer system having an object cache, a memory, and a translator *interposed* between the object cache and the memory, wherein the translator maps an object address to a physical address within the memory. Thus, the translator takes an object address as input and generates a physical address. The physical address may be subsequently used to retrieve one or more cache lines from memory. By having a translator interposed between the object cache and memory, an object address may be used by a processor and various levels of object caches (*e.g.*, L1 cache, L2 cache, etc) to request data.

In contrast, Henderson discloses a translator that takes a virtual address as input and generates a physical address. The physical address generated by the translator disclosed in Henderson is then used as a reference into an object cache. Further, Henderson teaches that the

physical address of a memory element is used to determine if a cache miss has occurred, thus *requiring* that the translator disclosed in Henderson is interposed between the processor and the object cache. Thus, Henderson provides a means for storing and accessing data in an object cache, however, fails to provide a means to interface the object cache and memory (col. 5, ll. 25-35). Further, Witt does not provide what Henderson lacks.

Specifically, Witt teaches the use of a translation look-aside buffers (TLB) to translate virtual addresses to physical address. The translation functionality of the TLBs allows processors as well as other functional units to communicate with the various caches in a multiprocessor system. However, Witt does not teach or suggest a translator that can translate between object addresses and physical addresses. Further, in contrast to the Examiner's assertion, Witt does not teach or suggest a translator interposed between cache and memory 1.

Regarding claims 19 and 28, the Examiner states that "Henderson does not explicitly teach translating the object address to a physical address if the object address is not in the tag array using a translator" as does the claimed invention. In fact, Henderson teaches away from translating object addresses to physical addresses only if the object address is not in the tag array. As explained above, Henderson teaches translation of a virtual address to a physical address on each processor memory access because memory elements stored in the object cache are accessed using the physical address. Hence, the virtual to physical translation in Henderson must be performed for each object cache access and not just on a cache miss.

In view of the above, claims 1, 19, and 28 are patentable over Henderson and Witt, whether considered separately or in combination. Dependent claims 2-9, 20-27, and 29-36 are likewise patentable for at least the same reasons. Accordingly, withdrawal of this rejection is

respectfully requested.

Claims 10-18 were rejected under 35 U.S.C. § 103 as obvious over U.S. Patent No. 6,446,188 ("Henderson") in view of U.S. Patent No. 6,240,484 ("Witt") and U.S. Patent Publication No. 2002/0178341 ("Frank"). This rejection is respectfully traversed.

The Examiner admits that neither Frank nor Henderson discloses "a translator interposed between the object cache and the memory" as required by claim 10. As explained above, Witt does not teach what Henderson and Frank lack. Therefore, claim 10 is patentable over Henderson, Witt, and Frank, whether considered separately or in combination. Dependent claims 11-18 are likewise patentable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 16159.072001).

Respectfully submitted,

Date: 2/19/04

#45,079

Jonathan P. Osha, Reg. No. 33,986
Rosenthal & Osha L.L.P.
One Houston Center, Suite 2800
1221 McKinney Street
Houston, TX 77010
Telephone: (713) 228-8600
Facsimile: (713) 228-8778

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